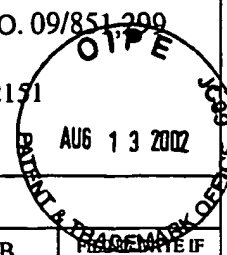


Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)			ATTY. DKT. NO. 5181-75400 APPLICANT: Lee, et al. FILING DATE: May 7, 2001		SERIAL NO. 09/851,200 GROUP: 2151		
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U.S. PATENT DOCUMENTS							
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATE IF APPROPRIATE
MD	B1	5,612,897	3/18/97	Rege			
MD	B6	5,862,312	1/19/99	Mann, et al.			

FOREIGN PATENT DOCUMENTS							
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
MD	B2	669 584	2/20/95	EP			
	B3	550 853	12/16/92	EP			
	B4	99/63442	12/9/99	WO			
	B5	646 858	8/26/94	EP			
	B2	669 584	2/20/95	EP			
	B7	99/17217	4/8/99	WO			
	B8	94/12939	6/9/94	WO			
	B9	439 693	8/7/91	EP			
✓	B10	92/06436	4/16/92	WO			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		

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Electronic Version v18

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Title of Invention	Routing Scheme Using Preferred Paths in a Mutli-Path Interconnection Fabric in a Storage Network																																									
<p>Application Number: 09/851299</p> <p>Confirmation Number: 3112</p> <p>First Named Applicant: Whay Lee</p> <p>Attorney Docket Number: 5181-75400</p> <p>Art Unit: 2151</p> <p>Search string: (4862496 or 5088032 or 5101480 or 5187671 or 5781534 or 6072774),pn.</p> <p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>WD</td><td>1</td><td>4862496</td><td>1989-08-29</td><td>Kelly et al</td><td rowspan="6"></td><td rowspan="6"></td><td rowspan="6"></td></tr><tr><td>WD</td><td>2</td><td>5088032</td><td>1992-02-11</td><td>Bosack</td></tr><tr><td>WD</td><td>3</td><td>5101480</td><td>1992-03-31</td><td>Shin et al</td></tr><tr><td>WD</td><td>4</td><td>5187671</td><td>1993-02-16</td><td>Cobb</td></tr><tr><td>WD</td><td>5</td><td>5781534</td><td>1998-07-14</td><td>Perlman et al</td></tr><tr><td>WD</td><td>6</td><td>6072774</td><td>2000-06-06</td><td>Natarajan et al</td></tr></tbody></table>		init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	WD	1	4862496	1989-08-29	Kelly et al				WD	2	5088032	1992-02-11	Bosack	WD	3	5101480	1992-03-31	Shin et al	WD	4	5187671	1993-02-16	Cobb	WD	5	5781534	1998-07-14	Perlman et al	WD	6	6072774	2000-06-06	Natarajan et al
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APPLICANT: Lee, et al.

FILING DATE: May 7, 2001

SERIAL NO. 09/851,299

GROUP: 2151

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
ND	A1	6,016,510	1/18/00	Quattromani, et al.			
	A2	6,023,753	2/8/00	Pechanek, et al.			
	A3	5,689,661	11/18/97	Hayashi, et al.			
	A4	6,167,502	12/26/00	Pechanek, et al.			
	A5	6,101,181	8/8/00	Passint, et al.			
	A6	5,720,025	2/17/98	Wilkes, et al.			
	A7	5,970,232	10/19/99	Passint, et al.			
	A8	6,055,618	4/25/00	Thorson			
	A9	5,701,416	12/23/97	Thorson, et al.			
	A10	5,737,628	4/7/98	Birritella, et al.			
✓	A11	5,689,646	11/18/97	Thorson			

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ND	A12	99/26429	5/27/99	WO			
ND	A13	0 785 512	7/23/97	EP			

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ND	A14	Bradley Kuzmaul, Mercury Computer Systems, Inc., "The RACE Network Architecture," (posted at www.mc.com/techlit/#tech_brief prior to this), 6 pages.					
ND	A15	R.Y. Wang, T.E. Anderson and D.A. Patterson, "Virtual Log Based File Systems For a Programmable Disk," Proc. Third Symposium on Operating Systems Design and Implementation, February 1999 (Also appeared as University of California Technical Report CSD-98-1031, 16 pages.					
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ND	A17	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Journal of the Association for Computing Machinery, Vol. 41, No. 5, September 1994, pp. 874-902.					

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	A19	Various Abstracts beginning with Funahashi, Jouraku and Amano, "Adaptive Routing for Recursive Diagonal Torus," Transactions of the Institute of Electronics, Information and Communication Engineers D-I, vol. J83D-I, no. 11, November 2000, pp. 1143-53.
	A20	Milan Kovacevic, Center for Telecommunications Research, "On Torus Topologies with Random Extra Links," IEEE 1996, pp. 410-418.
	A21	Dally, et al., The Torus Routing Chip, Distributed Computing, Springer-Verlag 1986, pp. 187-196.
	A22	Susan Hinrichs, "A Compile Time Model for Composing Parallel Programs," IEEE Parallel and Distributed Technology, 1995, 19 pages.
	A23	"CRAY T3D System Architecture Overview Manual," ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html, Cray Research, 1993, 40 pages.
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	A26	Dally, et al., "Architecture of a Message-Driven Processor," International Conference on Computer Architecture, June 1987, pp. 189-196.
	A27	Dennison, Lee and Dally, "High-Performance Bidirectional Signalling in VLSI," Massachusetts Institute of Technology, October 12, 1992, 20 pages.
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